Analysis of Symmetrical and Asymmetrical Cascaded H-Bridge Multilevel Inverters Using SPWM Technique

Muna Hassan Husien[1], Mohammed Ali AL-rawi[2]
[1]Department of Electrical Engineering ,Mosul University,Iraq.
[2]Department of Electrical Engineering ,Mosul University,Iraq
muna.20enp54@student.uomosul.edu.iq

Abstract

Multilevel inverters have gained popularity in high power, and medium voltage applications because they may be used without a transformer and with less noise and harmonic distortion. Multilevel inverters produce the stair-case voltage waveform close to the sinusoidal waveform by using a variety of DC voltage levels. The topologies of multilevel inverters (MLIs) are divided into three types: Diode Clamped, Flying Capacitor, and Cascade Multilevel Inverter (CMLI). CMLI topologies are classified into two types: symmetric and asymmetric topologies. The topologies of asymmetric cascade MLI comprise different DC sources but symmetric cascade MLI consists of equal DC sources. This paper presents a comparison between 9 symmetric MLI and 31 asymmetric MLI, and the technique of MCPWM is used to compare the two topologies. This study used two techniques from MC-PWM which are named Phase Disposition PWM, and Phase Opposition Disposition PWM. It has been discovered that the Phase Disposition PWM approach is more convenient in terms of Total Harmonic Distortion of output voltage in Asymmetric Cascade MLI, In general, an asymmetric topology at 31 levels was best than a symmetric topology at 9 levels. Using MATLAB / Simulink environment has been done to build models.

Keywords: Cascaded H-bridge multilevel inverter (CMLI), Multi carrier pulse width modulation (MC-PWM) technique, and Total harmonic distortion (THD), Phase Disposition PWM(PD-PWM), Phase Opposition Disposition PWM(POD-PWM), Asymmetric Cascade MLI (ACMLI).

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1. Introduction

Multilevel inverters are frequently utilized in high-power and high-voltage applications. The output waveform of a multilevel inverter is a staircase waveform that resembles a sinusoidal waveform[1,2]. Compared to the output voltage of a traditional inverter, the multilevel inverter has fewer harmonics. When the output of a multilevel inverter rises the inverter's number level to the N level, The output voltages have more steps, creating a staircase waveform with less harmonic distortion[3]. A large number of levels, however, complicates control and creates issues with voltage imbalance[4].

Following are the characteristics of multilevel inverters that are most appealing[5,6]:

- Able to provide output voltages with very little distortion
- Has little distortion when drawing input current.
- Produce a less common-mode voltage (CM), which lessens the strain on the motor bearings.
- Capable of operating at lower switching frequencies

Cascaded H Bridge multilevel inverter is also known as a multi-cell inverter. It is made up of a series of H-bridges[7]. Each H-bridge in the topology is supplied by an isolated dc source. Isolated dc sources include batteries, fuel cells, and ultracapacitors [7].The total output voltage is obtained by summing the voltages produced by each H-bridge connected to form a cascaded circuit. Each cell generates three voltage levels: positive, zero, and negative, by connecting a dc source to an alternating current output via various combinations of the four switches utilized in it [9].The CMLIs can be built using symmetric or asymmetric topologies.. In Asymmetric Cascade MLI, the voltage ratios of the sources' unbalanced DC sources increase as a power of two or three (ACMLI). The ACMLI topologies allow you to keep the same number of switching devices while increasing the output level.While symmetric Cascaded MLI ,the voltage same in every cell ,and the voltage increase by increasing number of cells[10,11].The symmetric CMLI and ACMLItopologies are shown in Figure(1).

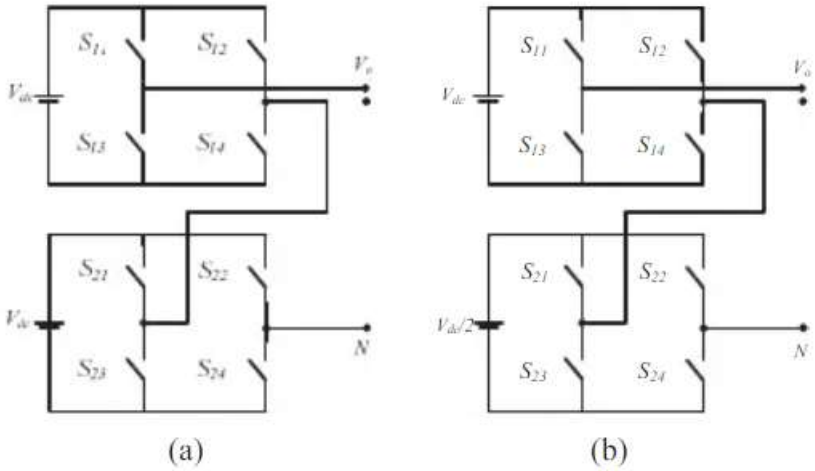

Figure 1. Cascaded H-bridge MLI topologies a) Symmetric b) Asymmetric

When each cell of the CHB-MLI is fed by the same amount of dc source, the structure is said to be symmetrical[10]. The magnitude of the dc source is expressed as[12].

VK=E……(1)

k=1,2,3.....m

V1=V2=.....Vm=E

In a symmetric multilevel inverter, the total number of output voltage levels n is given by

NL=2n+1…….(2)

Vm=nE

Asymmetric topologies are classified into two types: ACMLI and Asymmetric Hybrid MLI (AHMLI). The fundamental distinction between AHMLI and ACMLI is the switching devices. IGBT and MOSFET are two common semiconductors used in ACMLI to create H-Bridge cells[13]. However, in AHMLI topology, other semiconductors, including GTO, IGBT, and MOSFET, are used to make the cells[14].

If the ratio of DC sources in any asymmetric topology is twice that of the previous one, the topology is called a binary structure; if it is three times that of the previous one, the topology is called a trinary structure.

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Both (3) and (3) provide the output voltage level calculation for binary and trinary structures, respectively.

$$N_{binary} = 2^{n+1} - 1 \qquad V_{dc} = V / 2^{k-1}, k = 1, 2, \ldots, n \qquad \ldots\ldots\ldots 3$$

$$N_{trinary} = 3^{n} \qquad V_{dc} = V / 3^{k-1}, k = 1, 2, \ldots, n \qquad \ldots\ldots\ldots 4$$

Where:Nis the output voltage leveln is the cell number ,and k parameter is an integer.

2- Multi-Carrier PWM Methods for Multi-Level Inverters

MCPWM (Multi-Carrier PWM) employs a number of carrier waveforms. The number of carrier signals required for the N-level inverter is (N-1)[14]. PhaseShifted PWM (PSPWM) and Level Shifted PWM are subtypes of the multi-level Sinusoidal PWM or (MCPWM) . LSPWM classified into three types: Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM), and Alternate Phase Opposition Disposition PWM (APODPWM) (APODPWM)[15,16].

- A sinusoidal reference signal is compared to (N-1) number of carrier signals in Phase Disposition PWM (PDPWM). In 9-level is needed Eight carriers and one reference signal inverter[17]. All of the carrier signals are in phase and of similar magnitude,as illustrated in Fig. 2

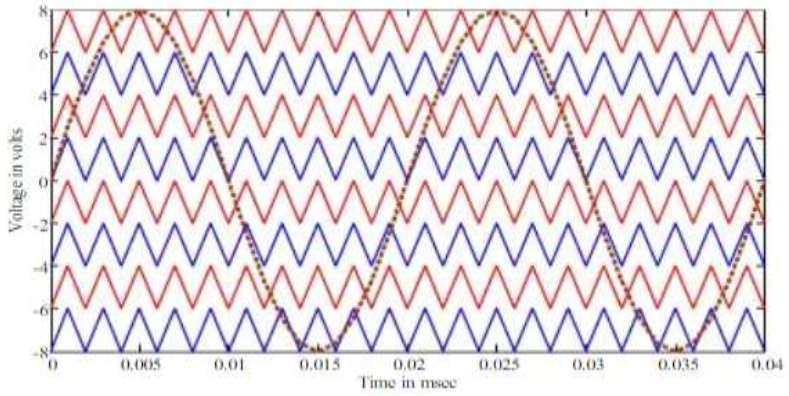

Fig2 Reference and carrier waveforms for PD-9 level

- In Phase Opposition Disposition PWM (PODPWM), a (N-1) number of carrier signals and a sinusoidal reference signal are compared. Above zero reference values, the carrier signals are in phase. , the carrier signals below zero level are 180° out of phase with them[18]. In order to create a 9-level inverter, eight carriers and one reference signal are needed see (Fig. 3).

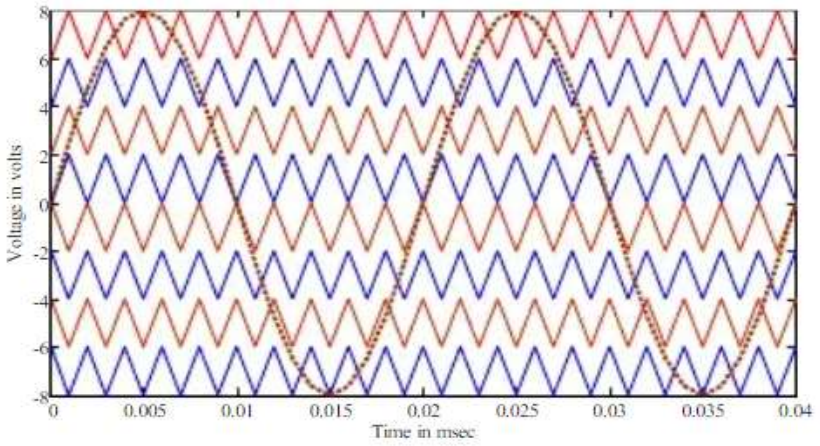

Fig3. Reference and carrier waveforms for POD-9 level

- Alternate Phase Opposition Disposition (APODPWM) additionally needs (N-1) carrier signals .The carrier signals must alternately be 180° out of phase with one another[19]. The carrier and reference waveforms for the 9-level inverter's PODPWM are shown in Fig. 4

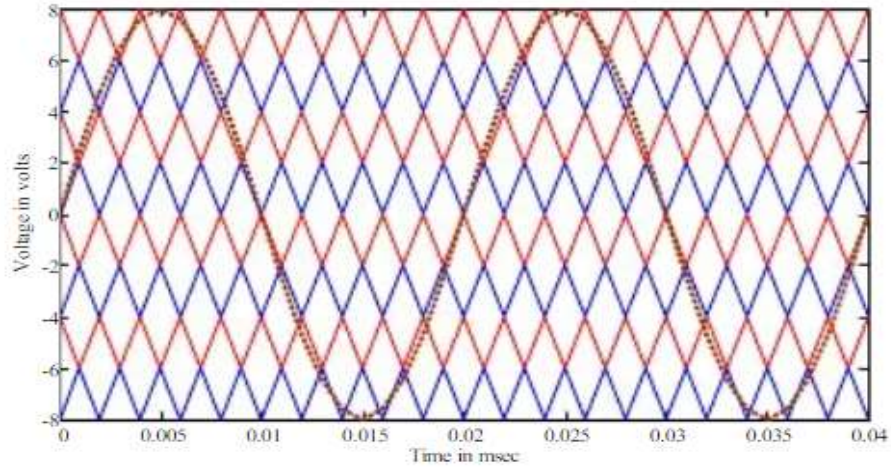

Fig4. Reference and carrier waveforms for APOD-9 level

3-Simulation results

A)THD analysis of 9-level SMLI

In MATLAB/SIMULINK, a nine-level, symmetric cascaded multilevel inverter with R load was simulated with solver ode23t.The block diagram of nine-level SMLI is given in Figure(5).Where Four cells with equal voltages were used and R value is 100connected to the output of theinverter.In an n-level inverter, (n-l) carriers are employed to compare

with the modulation signal in MC-PWM.There are eight triangular carrier signals for nine-level SMLI inverter in the MC-PWM [20].

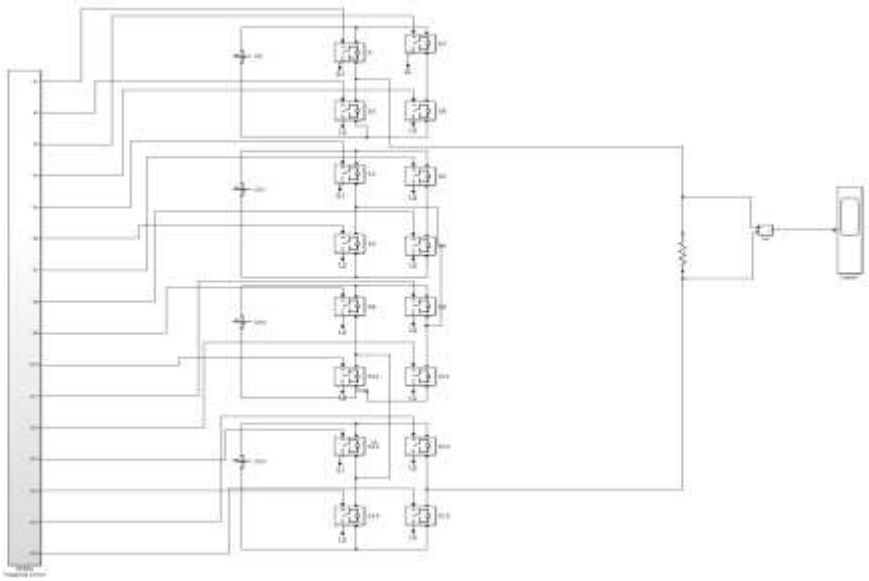

Figure 5. nine level multilevel inverter module

The FFT analysis for output voltage waveform using PD-PWM is shown in Fig. 5 . Figure 6 depicts the FFT analysis for voltage waveform utilizing POD-PWM [21].

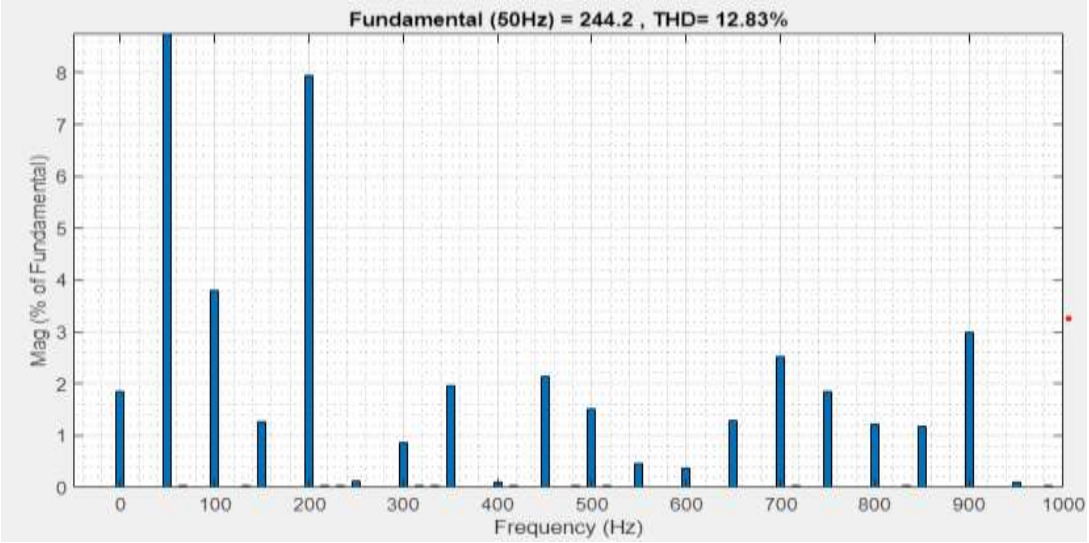

Fig.5 FFT analysis of voltagewaveform of 9-SMLI using PD-PWM

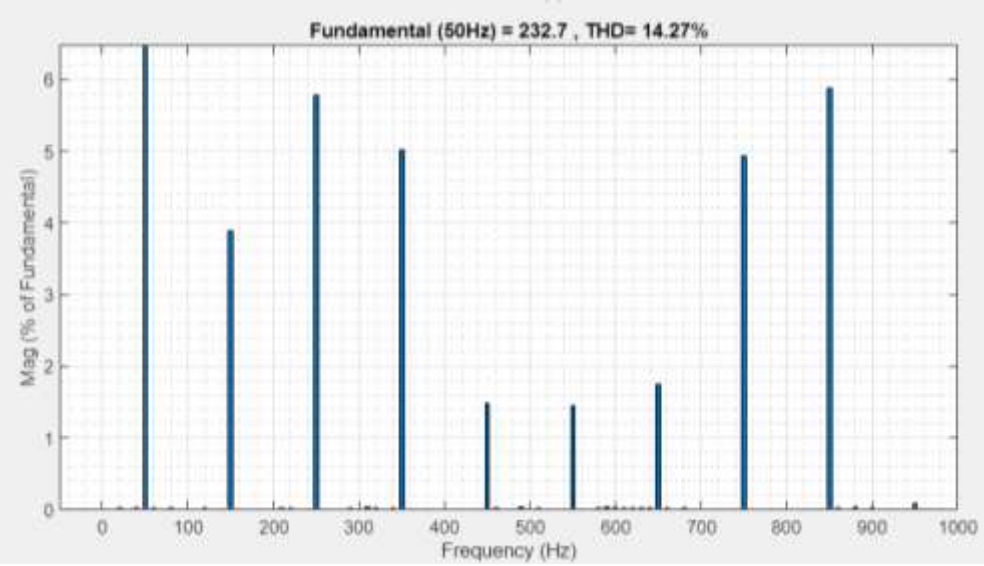

Fig .6 FFT analysis of voltagewaveform of 9-SMLI using POD-PWM

B)THD analysis of 31-level AMLI

In this study, a31-level ACMLI topology is used with binary structure. Four H-bridge cells are linked in serial, and the supply voltages are used as VDC1=21,VDC2=42,VDC3=84 and VDC4=168.Also used MATLAB/SIMULINK to build the circuit of 31 level symmetric cascaded multilevel inverter with R load as shown in figure (7)[22] .

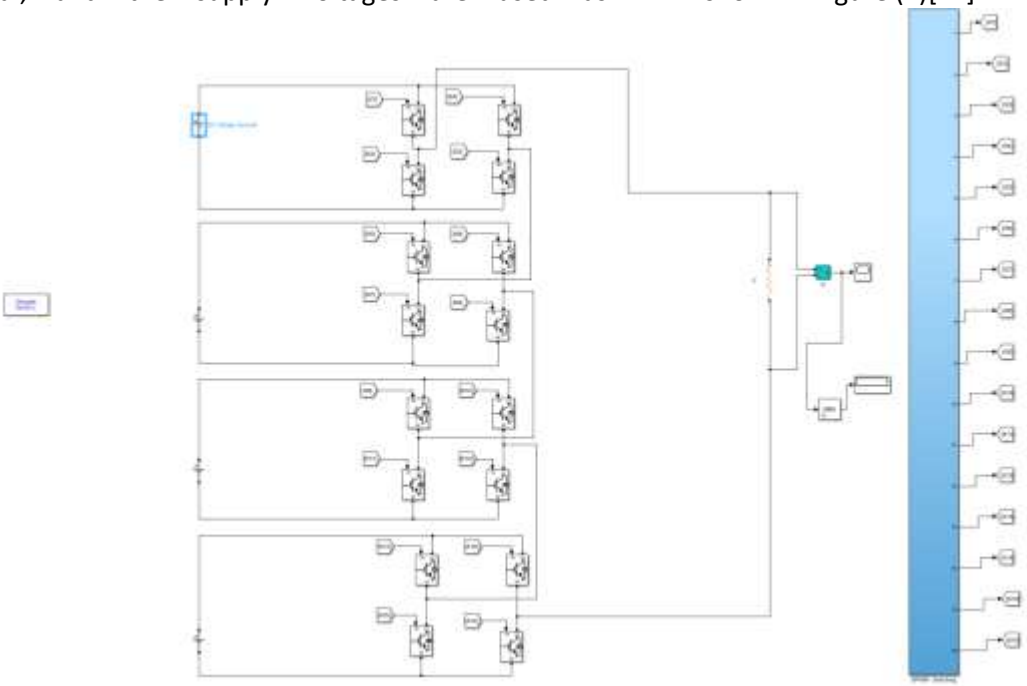

Figure 7. 31 level multilevel inverter module

FFT analysis was used to determine the output voltage's THD content.THD analysis of 31-levels AMLI by using PD-PWM and POD-PWM are given below.

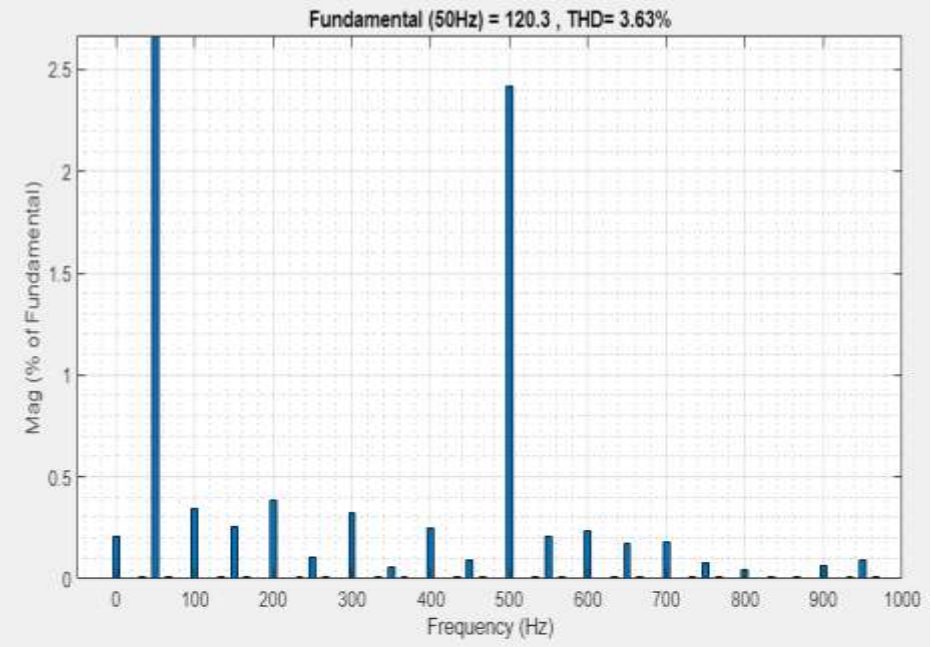

Figure .8 FFT analysis of voltagewaveform of 31-AMLI using PD-PWM

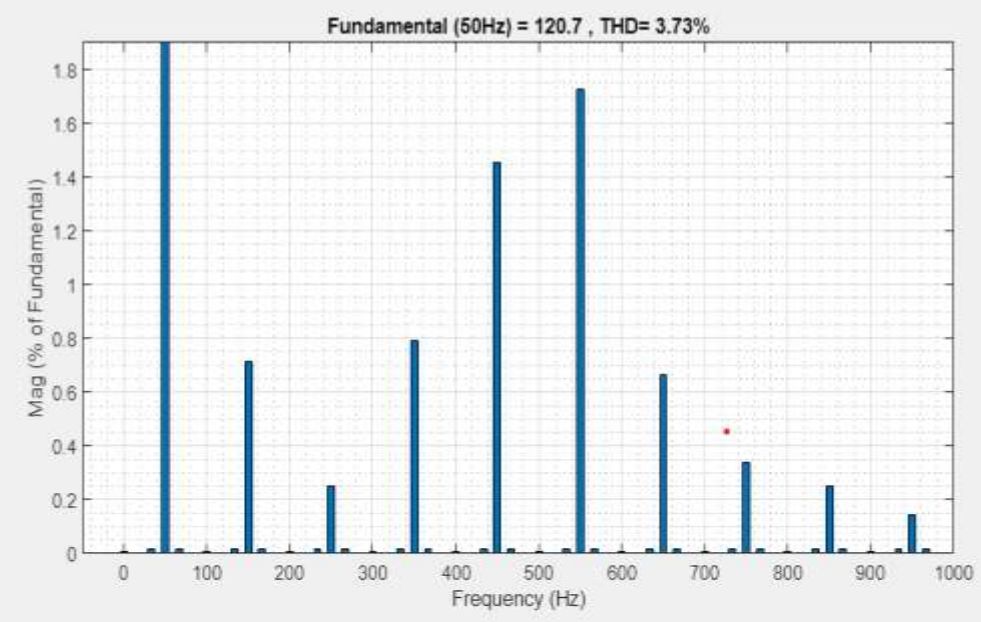

Figure .9 FFT analysis of voltagewaveform of 31-AMLI using POD-PWM

Table1 :comparison of performance Parameters of 9-levelSymmetric and31-level Asymmetric CHB Inverter

Parameters	symmetric inverter	Asymmetric inverter

Number of dc sources	4	4
Number of switches	16	16
Fundamental frequency	50	50
Carrier frequency	1KHZ	1KHZ
Voltage levels	9	31
Voltage THD in PD-PWM	12.83	3.63
Voltage THD in POD-PWM	14.27	3.73
Voltage THD in APD-PWM	10.96	3.59

4-Conclusion:

This paper deals with a comparison of a Symmetrical 9-level and asymmetrical 31-level Cascaded H-Bridge multilevel inverter with a resistive load with four H-bridges. The simulation results show that the generated voltage spectrum for the Asymmetric multilevel inverter design is better than a symmetric multilevel inverter. where uses the same amount of switches and dc sources like symmetric but produces voltage with the fewest harmonics. It has been determined that AsymmetricalCMLI, in general, is the best choice of MLI in terms of component requirements, with fewer THD observed for this topology. The THD of the voltage of both converters was tested using several SPWM modulation techniques such as PD and POD, with the PD-PWM methodology exhibiting the lowest THD.

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