



# Design of Low Power CMOS RF Tx used for IEEE 802.15.4

Dr.D.Manikya.Krishna chaitanya<sup>1</sup>, Sri lakshmi Aouth<sup>2</sup> Dr.Farha Anjum<sup>3</sup>,Dr.mohammad Iliyas<sup>4</sup> A. sindhuja<sup>5</sup>

<sup>1</sup>Assoc Professor of ECE Dept,Vasavi college of Engineering, Hyderabad,India

<sup>2</sup>Assoc Professor of ECE Dept,Vasavi college of Engineering, Hyderabad,India

<sup>4</sup> Professor of ECE Dept,HOD, Shadan college of engineering of Engineering and Technology Hyderabad,India

<sup>3</sup> Professor of ECE Dept,HOD, Siddhartha Institute of Engineering and Technology,Ibrahimpatnam Hyderabad,India

<sup>5</sup> Assistant professor of ECE Dept, Sri Indu institute of Engineering and Technology,hyd,India

farha.ece@gmail.com,chaitanyadm@gmail.com,srilaxmi1108@gmail.com,ilyas.ece@gmail.com  
,sindhu4b3@gmail.com

## ABSTRACT

IEEE 802.15.4 is a network maintained by the IEEE 802.15 work group. CMOS RF transmitter is widely used in the latest wireless communication systems. CMOS RF transmitter will use both MOS technology and RF. RF CMOS circuits are widely used for transmitting and receiving the wireless signals. RF CMOS technology is widely used for WLAN networks. RF CMOS technology also used in radio transmitters and receivers such as GSM, WIFI etc. CMOS devices have high noise immunity and low power consumption. Hence they are widely used for IC's. Here work gives the objective solutions of a low power Radio Frequency Tx for 2.4GHz band

IEEE 802.15.4 standard in 0.18 $\mu$ m CMOS. For an adaptive Radio Frequency Tx, more elements are admired. The important influential elements here are executions, energy utilization, product energy, and price. Radio Frequency Tx has a nonresistant mixers, and a power amplifier. This aimed Radio Frequency Tx needs simply 10.8mW under a force voltage of 1.8 Volts, deliver of 2 Volts.

**Key terms:** Complementary Metal Oxide Semiconductor, Power Reduction, WSN, IEEE standard 802.15.4 Tx.  
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## 1. Introduction

New increase of reduced power Complementary Metal Oxide Semiconductor transmitters and receivers of 2.4GHz in furrowing drastically with the origin of the IEEE802.15.4 (1).

IEEE 802.15.4 needs a good backup and low price answers in favor of operations. This set indicates the high level consumption of tiny, cheap, and high backup scenting genius called detector knot by on panel dispensation and wireless communication capacities which reach a

complexion-arranged, infrastructure less, and fault tolerant detector network within concerted manner. By connate system, 3 working frequency bands available 868MHz European, 915MHz America, and 2.4GHz widely. There are three possible data rate of the this standard based upon the working bands they are 20 kbps, 40 kbps and 250 kbps. IEEE 802.15.4 stationed for more days of time in a broad variety of implicit operations screenplays, like mechanization, refined, home electronic products, patented personal care, and



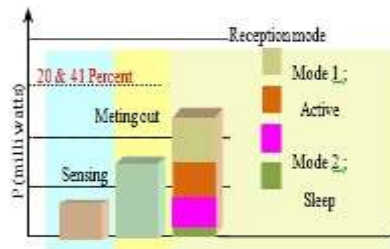
consanguineous miracles. In line, energy utilization is a elemental issue to achieve demanded system duration as battery change of detector knots was hourly insolvable.

This Sub System needs above 50% of power at the time of processing. This design of a RF front unit in favor of Wireless Sensor Networks results the transmitter unit is one of the most power-consuming components. As a result of improving power utilization, overall utilization & power needs our Radio Frequency components developed immensely. So, here we set goal the Tx plan to reduce the power expenditure. Here the intend & execution of a low power CMOS Radio Frequency tx for IEEE-802.15.4 has unique target of minimum power, Lower distortion, and More Uniqueness, In our method, a passive mixer

operating in present scenario is paired with an Booster Amplifier [2]. Remaining work is illustrated below.

## 2. Related Work

Recently, there have been several low-power CMOS based 2.4-GHz transmitters and receivers of IEEE 802.15.4 [3]. Unfortunately, these works do not serve IEEE 802.15.4 applications well in terms of energy efficiency. These search results, however, silently scatter more power rakishness. Accordingly, it is advantageous to reduce the power rakishness. The most common solution to address the above concerns is to use a current reused method [4]. This method has a limited increase because of the queue of more transistors.



**Fig 1. Sharing of power utilization Using processing and transferring.**

Fig 1. Shows the power utilization using processing and transferring modes. There are two modes of operation namely Active mode and Sleeping mode. Y axis shows the power utilization in milli watts. The sensing , Meeting and percentage is shown in fig 1. Transmitter and Receiver designs of WSN are of 3 types: 1. Super heterodyne 2. Small transitional frequency 3) Straight translation (5). Super heterodyne architectures require many combiners, resulting in greater power and complicating transceiver implementations. Low-IF architectures are divided as per large ADC sample speed, which leads to more power utilization. [6]. Direct conversion type uses a min no. of exterior devices, like IR filter, it is unnecessary & an Intermediate Frequency BPF is adjusted by the LPF.

In this design, the direct-conversion scheme is taken from a minimum price and minimum energy perspective. The minimum power utilization and minimum development prices of direct conversion type, as well as its effortless assimilation among the design, make it attractive. With the low-IF

receiver, the image signals are rejected in the transmitter chain. As the phase changer is intrinsically thin band this architecture uses a 90 degrees phase changer in the gesture line which limits signal bandwidth. Transmitter under consideration has a quad inactive mixer & a tiny noise power amplifier.

In this type, an o/p Radio Frequency signal from the up switch mixer is then improved by a usual cascade technique through an extra condenser C1 as given at fig 3. Power amplifiers enable a signal to be transmitted with the necessary output power. It is necessary to add a capacitor to input end of the i/p-transistor M1 in order to maintain proper i/p line straight, as the C1 is basically a bias reliant, can rise to small noise at soaring i/p booster levels-(8). Here i/p-transistor is influenced with a large -Gate-Source voltage to run in Group A method. This amplifier has current utilization of 6 mA at 1.8V.

The above method is used because of below advantages:

- High power boundary, linearity can be



increased.

- The gain is restricted by changing the Direct Current of the P type Metal Oxide

With this Power Amplifiers, the set-up  $L_1 - C_1$  removes the 2<sup>nd</sup> order of the transporter, while the set-up  $L_2$  &  $C_2$  set at transporter frequency. The  $Z_{in}$  of the planned Power Amplifier as shown below,

$$Z_{in} = \frac{1}{j\omega L(C_{gs} + C_1)}$$

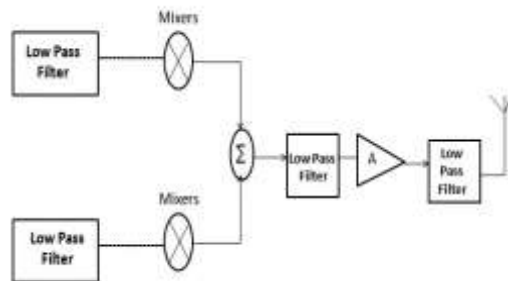
Here,  $C_{gs}$  is gate-source capacitance,  $L$  is inductance,  $C_1$  is the capacitance. The set-up  $L_2 - C_2$

Our standard utilities have a small duty factor because of this architecture. Thus, it's important for minimizing their utilization both in action type and while sleeping. A 1 micro amp power supply is

Semiconductor by altering direct voltage to cascode transistor input.

is used to set the output impedance to 50 Ohms.

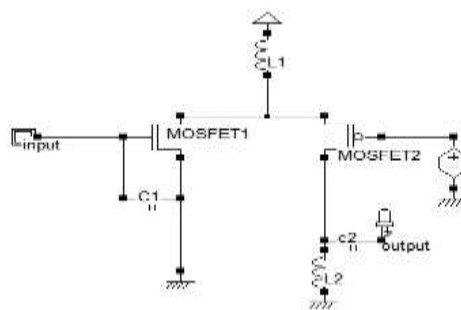
required for the latter mode. Consequently, a small silicon surface and small no. of exterior mechanisms are essential for reducing the cost of such circuits.



**Fig 2. Schematic of Tx Radio Frequency Amplifier**

Figure 2. Shows the schematic diagram of a transmitter radio frequency amplifier. It uses two low pass filters. The outputs of two low pass filters are connected to two mixers. Now the output of two mixers added by an adder. The

output of a adder is passed through the low pass filter then amplified by an opamp. Now at final the amplified signal is filtered by a low pass filter. Then it is transmitted by an RF antenna.



**Fig 3. Power Amplifier**

Fig.3 shows the power amplifier. It uses two MOSFET's namely MOSFET1 and MOSFET2. It uses two capacitors namely C1 and C2. It uses two inductors which are named as L1 and L2. Input is

applied to MOSFET1 and the amplified output is collected from MOSFET2.

**3. Simulation Results and Discussions**



ADS simulation tools are used to simulate the circuit in- 0.18-m Complementary Metal Oxide Semiconductor. Route has planned for 2.4-GHz In System the 2.4 - 2.48 GHz b/w is used. 1.8 Volts gives 6 mA on the Tx. -S-parameters of the PA is given at Fig.4. I/P and O/P combination are efficient in the required IF = 6 MHz . From

Fig.4(a) and (b) it is clear the i/p & o/p resistance of the planned Power Amplifier is finely achieved at 2.4 GHz. The output power signal is

used to determine the transmission reliability as the sensor setup is utilized for few serious sensing applications. The O/P shows that the designed plan reduces extensively the power utilization.

Here we offer a judgment of the O/P of this plan with the various studies in **Table 1**. In **Table 1**, this plan has tiny power dissipation but obtaining good performance compare to others.

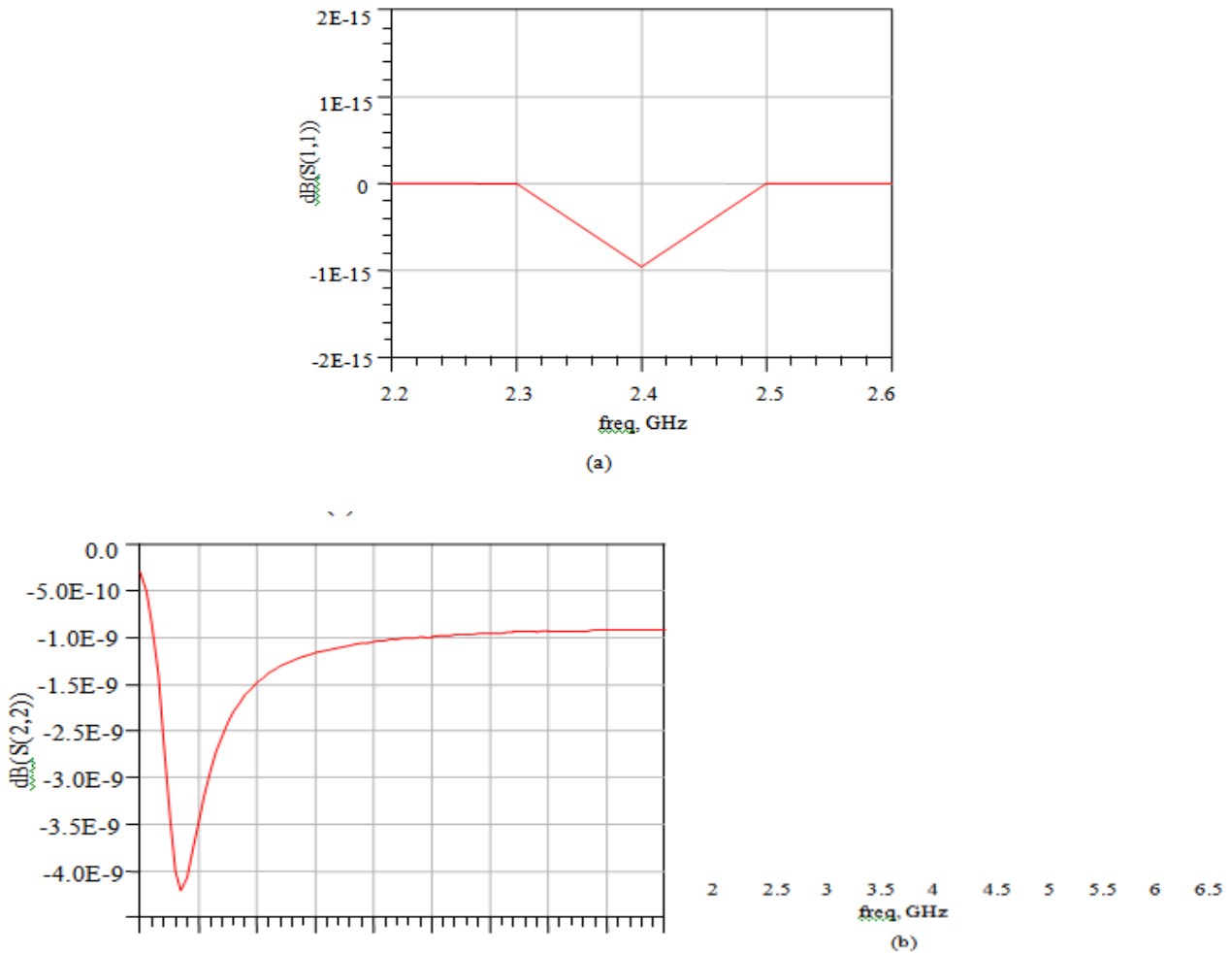


Fig 4. S-parameters (1) I/P return loss (S<sub>11</sub>) (2) Reverse isolation (S<sub>22</sub>).

| Parameters            | [10] | [11] | [12] | [13] | This Work |
|-----------------------|------|------|------|------|-----------|
| CMOS Technology(μm)   | 0.25 | 0.18 | 0.18 | 0.18 | 0.18      |
| Output Power(dBm)     | 0    | 0    | -4   | 0    | 1.7       |
| Power Dissipation(mW) | 12   | 18   | 17   | 25   | 10.8      |
| Architecture          | SHD  | DCT  | DCT  | DCT  | DCT       |



### Table.1 Performance Comparison

#### 4. Conclusion

2.4 GHz CMOS Radio Frequency Transmitter for IEEE 802.15.4 with reduced power has been planned in this work. Then the provisions for the sensitive unit, which is the power amplifier, were given. At a voltage of 1.8 Volts, transceiver was manufactured in 0.18  $\mu$ m technique. The PA showed an increased competence of 38.8% & rakishness of 9 milli Watts. Here entire  $T_x$  sequence, 1.7dBm of O/P power & 3.98 dBm of O/P 3<sup>rd</sup> order cut off point is achieved. According to planned  $T_x$ , it dispensed 10.8 mill Watts.

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